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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,519	11/17/2003	Simon Charles Watt	550-480	6837

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EXAMINER	
ABEDIN, SHANTO	

ART UNIT	PAPER NUMBER
2136	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,519	WATT ET AL.	
	Examiner	Art Unit	
	Shanto M Z Abedin	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/17/2003,09/16/2004*, 01/16/2007
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the communication filed on o4/20/2004.

2. The information disclosure statement received on 11/17/2003, 09/16/2004 and 01/16/2007 have been considered, and the signed copy of the IDS' have been sent to the applicant with this office action.

3. Formal drawings submitted on 04/20/2004 have been accepted.

4. The examiner acknowledges that this application claims priority to a foreign application filed earlier on 11/18/2002, and the certified copy of the foreign application is received and accepted.

5. Claim 1-47 were currently presented for the examination.

6. Claim 1-47 have been rejected.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

7. The abstract of the disclosure is objected to because (a) it is written in more than one paragraph, and (b)" [Figure 10]" at the end of the abstract seems to be unnecessary. Correction is required. See MPEP § 608.01(b).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-47 are provisionally rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1- 67 of copending application no. 10/714518.

Regarding claims 1 and 24, they are unpatentable over claims 1, 8, 12, 17-22, 34 and 53-56 of copending application no. 10/714518.

Regarding claims 2-8 and 25-31, they are unpatentable over claims 4-16 and 38-45 of copending application no. 10/714518.

Regarding claims 9-10 and 32-33, they are unpatentable over claims 1-4, 19-20, 34-38 and 52-54 of copending application no. 10/714518.

Regarding claims 11-23 and 34-47 they are unpatentable over claims 23-33 and 56-67 of copending application no. 10/714518.

Although the conflicting claims are not identical, they are not patentably distinct from each other because all the elements/ features of claim-set of the instant application either exist in similar or different names, or being obvious by the conflicting claim-set of the copending application no. 10/714518. This is a provisional obviousness –type double patenting rejection because the conflicting claims have not in fact been patented.

9. Claims 1-8 and 24-31 are provisionally rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-17 of copending application

no. 10/714563 for the reasons already stated in earlier paragraph. This is a provisional obviousness –type double patenting rejection because the conflicting claims have not in fact been patented.

10. Claims 1-8 and 24-31 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-3 and 8-10 of prior commonly assigned U.S. Patent No. 7124274B2 for the reasons already stated in earlier paragraph.

This is a double patenting rejection.

11. Claims 1-8 and 24-31 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-11 of prior commonly assigned U.S. Patent No. 7117284 B2 for the reasons already stated in earlier paragraph.

This is a double patenting rejection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 24-47 are rejected under 35 USC 101 because of being directed to non-statutory subject matter.

Regarding claims 24-27, they are directed to computer program product, or executing a program, therefore, they raise a question whether the claimed method is carried out through an executable program/ software package/ driver or not, and subsequently, they are rejected as being non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1- 10, 12-18, 21-33, 35-41 and 44-47 are rejected under 35 USC 102 (e) as being anticipated by Christie et al (US 7165135 B1).

Regarding claims 1 and 24, Christie et al discloses apparatus/ method for processing data, said apparatus/ method comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) said plurality of modes including:

at least one secure mode being a mode in said secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) ; and

at least one non-secure mode being a mode in said non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, normal mode and domain);

wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode (Col 4, starting at line 65; Col 10, starting at line 31; Claim 1)

said processor is responsive to one or more exception conditions for triggering exception processing using an exception handler, said processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Col 4, starting at line 7; Col 10, starting at line 31; Claim 1-9) .

Regarding claim 2, Christie et al discloses apparatus wherein at least one of said exceptions is a selectable exception handled by a selectable one of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode; and at least one of said exceptions is a dedicated secure exception that is handled by a secure exception handler operating in a secure mode (Col 9, starting at line 45; Claim 2; exception handling logic).

Regarding claim 3, Christie et al discloses apparatus wherein said one or more exception conditions can be programmably configured to trigger either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Col 9, starting at line 45; Claim 1-9; calling exception handler).

Regarding claim 4, Christie et al discloses apparatus having a secure exception is triggered by one of a signal on a dedicated secure exception signal input and a non-secure exception signal input (Col 9, starting at line 45; Claim 1-9).

Regarding claim 5, Christie et al discloses apparatus having an exception signal input shared between secure and non-secure exceptions and a further input signal cooperating with said

exception signal input to control whether a secure exception handler or a non-secure exception handler is triggered (Col 9, starting at line 45; Claim 1-9).

Regarding claim 6, Christie et al discloses apparatus wherein said secure exception handler is part of a secure operating system operable in said secure mode (Col 9, starting at line 45; Claim 1-9).

Regarding claim 7, Christie et al discloses apparatus wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (Col 9, starting at line 45; Claim 1-9).

Regarding claim 8, Christie et al discloses apparatus wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception takes place via said monitor mode, said processor being operable at least partially in said monitor mode to execute a monitor program to manage switching between said secure mode and said non-secure mode (Col 2, starting at line 26; Col 5, starting ln 30).

Regarding claim 9, Christie et al discloses apparatus wherein said monitor program is operable to save and restore context data defining processor status when switching between a secure mode and a non-secure mode to handle an exception (Col 2, starting at line 26; Col 5, starting at line 30; Col 10, starting at line 31).

Regarding claim 10, Christie et al discloses apparatus wherein said processor includes a register bank and said monitor program is operable to flush at least a portion of said register bank shared between said secure mode and said non-secure mode when switching from said secure mode to said non-secure mode such that no secure data held within said register bank may pass from said

secure mode to said non-secure mode other than as permitted by said monitor program (Col 7, starting at line 31; memory bank) .

Regarding claim 12 , Christie et al discloses apparatus wherein said processor is responsive to an exception condition to select an exception handler in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition; and said active exception vector table is one of a plurality of exception vector tables (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45; exception handling logic).

Regarding claim 13 , Christie et al discloses apparatus wherein said plurality of exception vector tables include a secure exception vector table selectable in said secure mode and a non-secure exception vector table selectable in said non-secure mode (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45; exception handling logic).

Regarding claim 14 , Christie et al discloses apparatus wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode said plurality of exception vector is performed via said monitor mode (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45).

Regarding claim 15, Christie et al discloses apparatus wherein said plurality of exception vector tables include a monitor mode exception vector table (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45).

Regarding claim 16, Christie et al discloses apparatus wherein said processor is responsive to one or more parameters specifying which of said exceptions should be handled by said monitor mode exception vector table (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45).

Regarding claim 17, Christie et al discloses apparatus wherein said secure vector table is said active vector table in said secure mode and said non-secure vector table is said active vector table in said non-secure mode unless said one or more parameters specify that said monitor mode vector table is said active vector table of said exception condition (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45).

Regarding claim 18, Christie et al discloses apparatus wherein at least one of said parameters is stored in an exception trap mask (Col 8, starting at line 33; Col 10, starting at line 40; memory for exception/ interrupt handling).

Regarding claims 21-23,25-33, 35-41 and 44-47, they recite the similar limitations that already addressed rejecting claims 1-10, 12-18 and 24, therefore, claims 21-23,25-33, 35-41 and 44-47 are rejected applying as above rejecting claims 1-10,12-18 and 24.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 11, 19-20, 34 and 42-43 are rejected under 35 USC 103 (a) as being unpatentable over Christie et al (US 7165135 B1).

Regarding claims 11 and 34, Christie et al fails to disclose wherein said exception conditions includes one of more of: a secure interrupt signal exception; a mode switching software interrupt signal; a reset exception; an interrupt signal exception; a software interrupt signal; an undefined instruction exception; a prefetch abort exception; a data abort exception; and a fast interrupt signal exception.

The examiner takes official notice that above mention exceptions are well known in the art, therefore, it would be obvious to a person of ordinary skill in art to design the method further including one of more of above exceptions in order to provide multiple exception choices.

Regarding claims 19-20 and 42-43, Christie et al fails to disclose exception trap mask register is non-writable when said processor is not in non-secure domain. However, at the time of invention, it would be logically obvious to ordinary skill in art to design the exception handling registers such a way that it is non-writable when processor is in a secure domain (or not in a non-secure domain) in order to provide a better memory level access control mechanism.

Conclusion

15. A shortened statutory period for response to this action is set to expire in 3 (Three) months and 0 (Zero) days from the mailing date of this letter. Failure to respond within the period for response will result in ABANDOMENT of the application (see 35 U.S.C 133, M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shanto M Z Abedin whose telephone number is 571-272-3551. The examiner can normally be reached on M-F from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moazzami Nasser, can be reached on 571-

272-4195. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shanto M Z Abedin

Examiner, AU 2136

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4/30/07